

FIG. 1

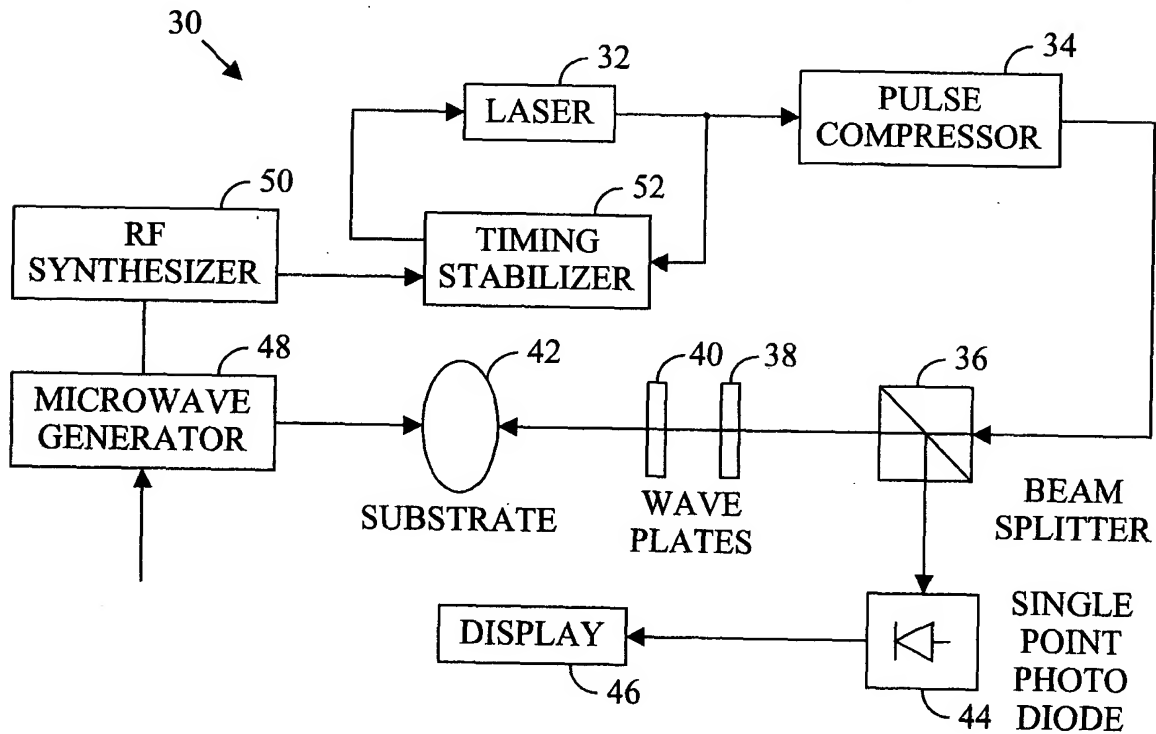


FIG. 2

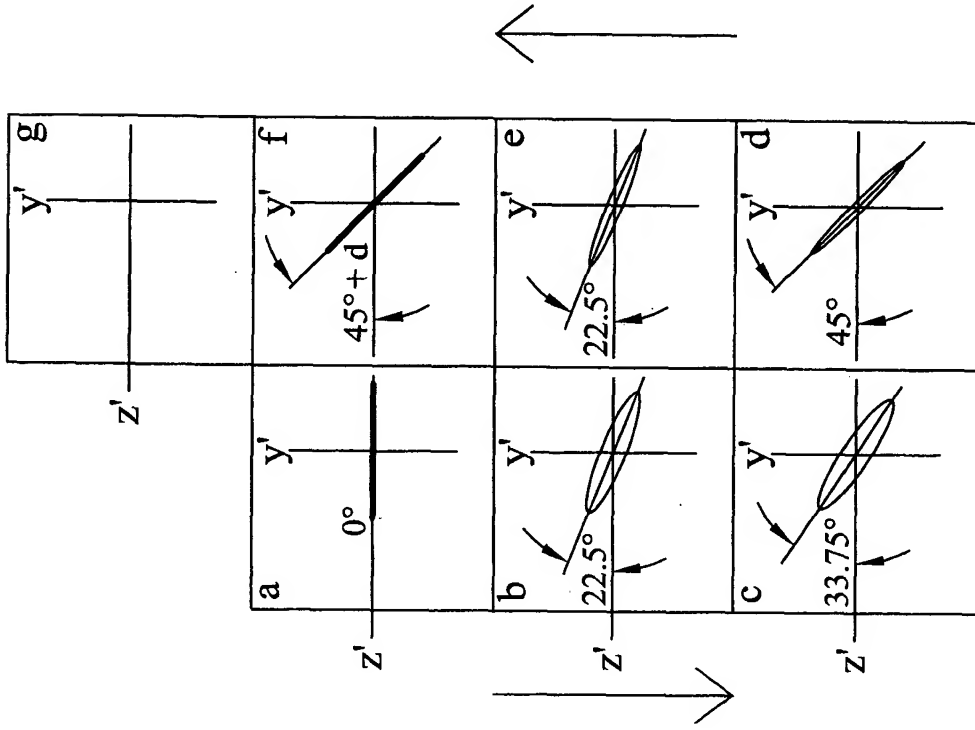


FIG. 3B

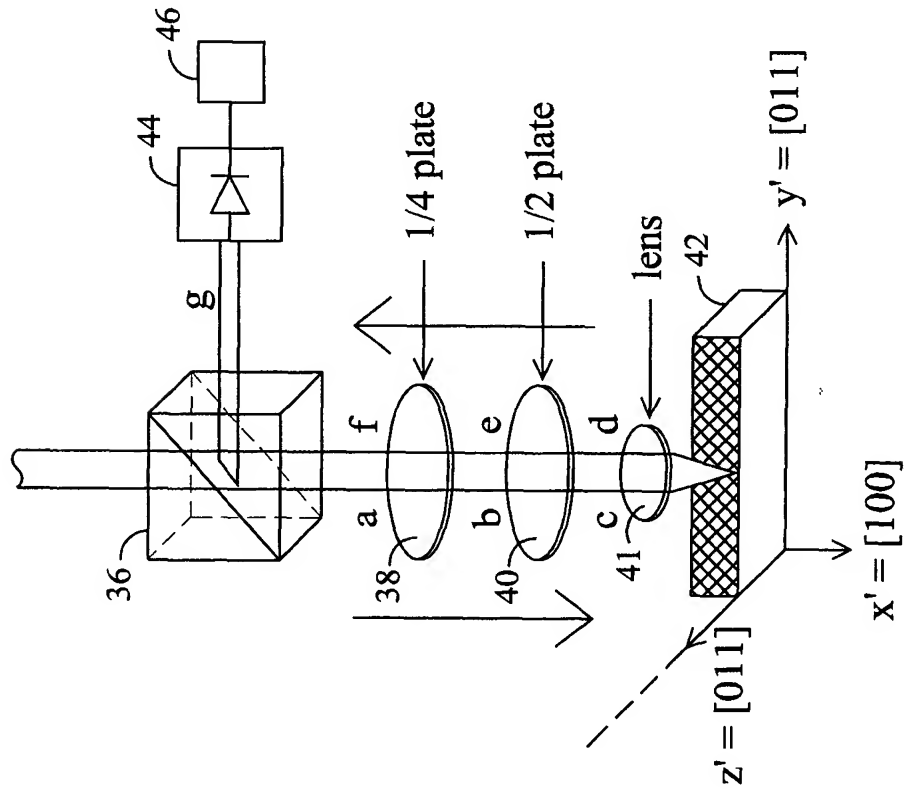


FIG. 3A

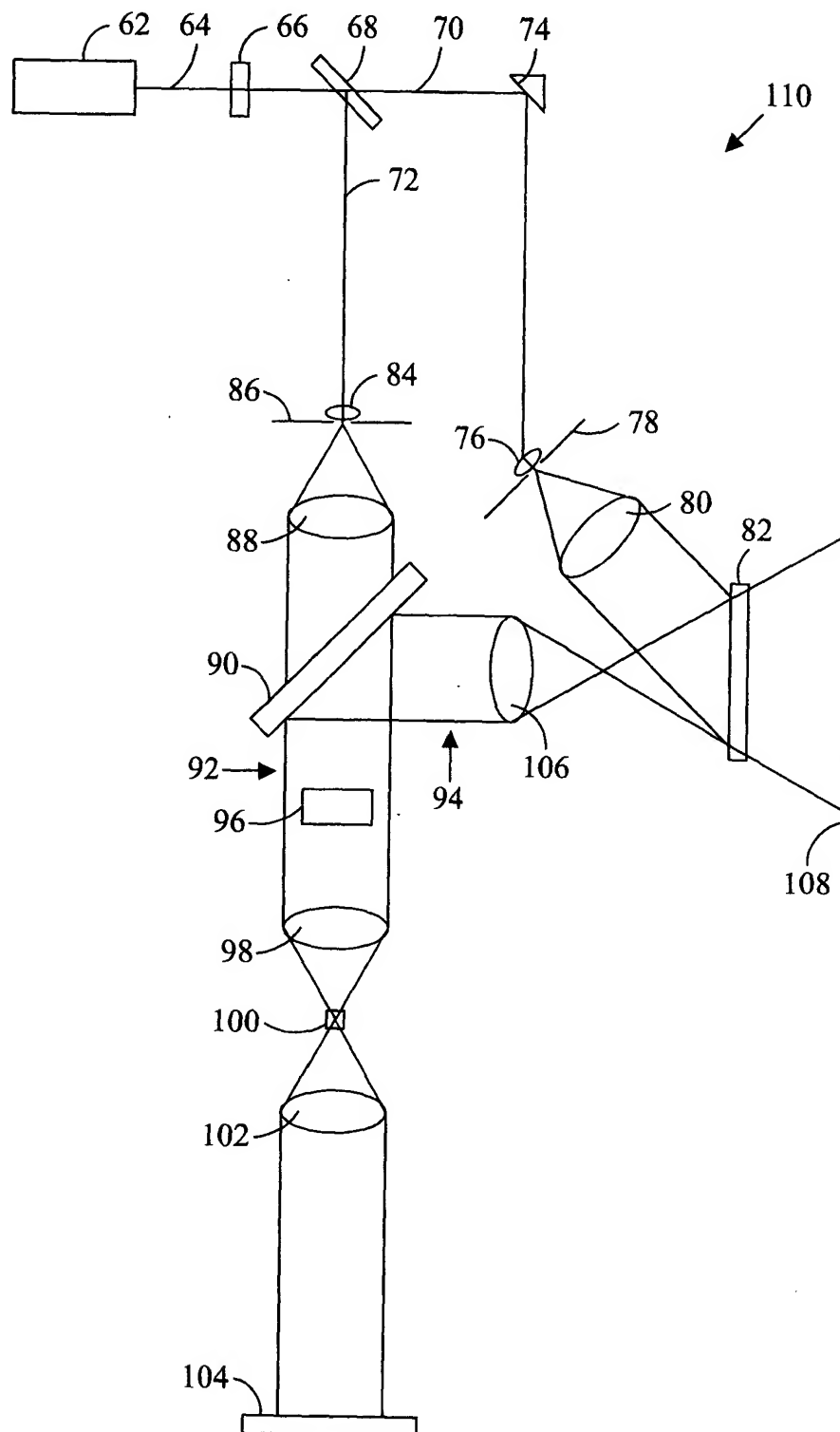


FIG. 4

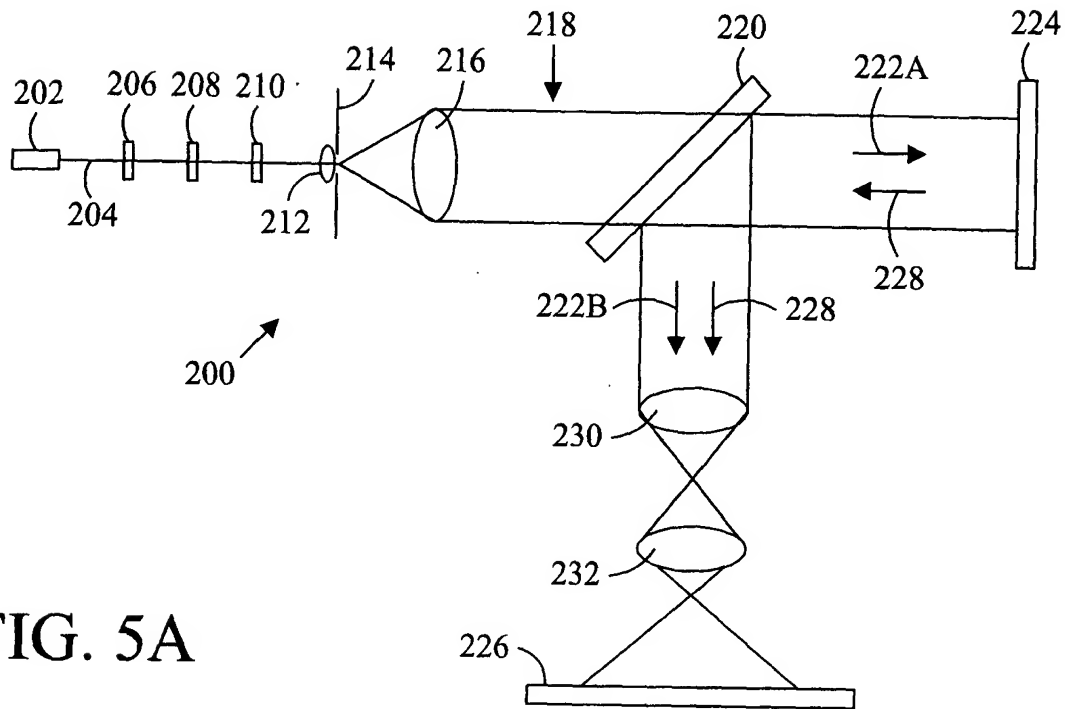


FIG. 5A

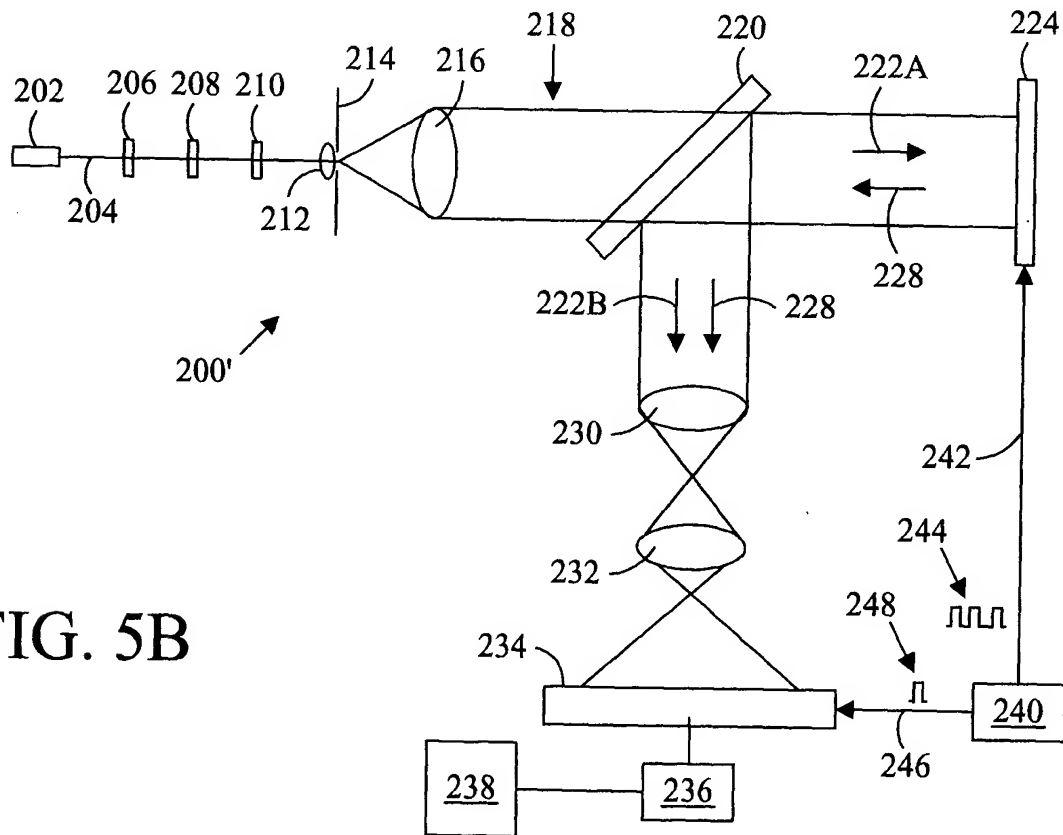


FIG. 5B

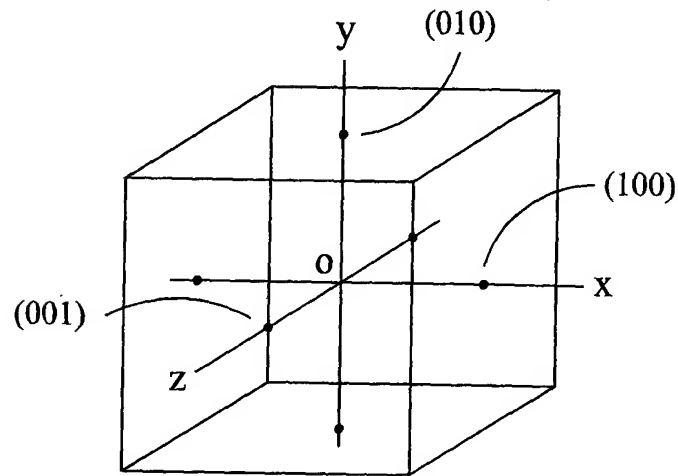


FIG. 6A

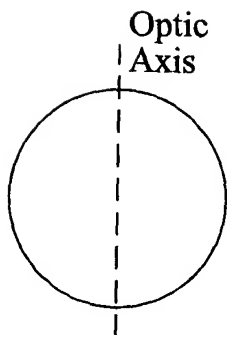


FIG. 6B

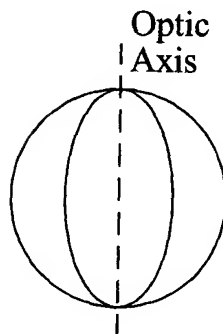


FIG. 6C

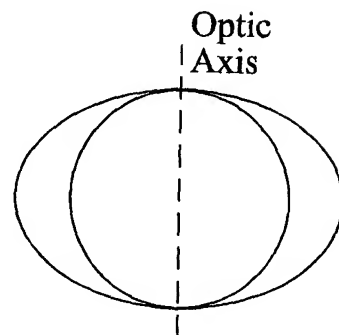


FIG. 6D

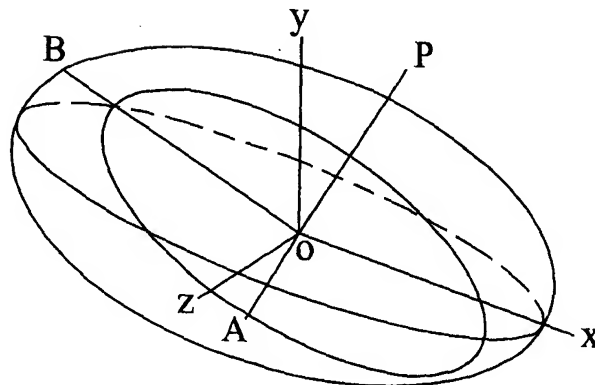


FIG. 6E

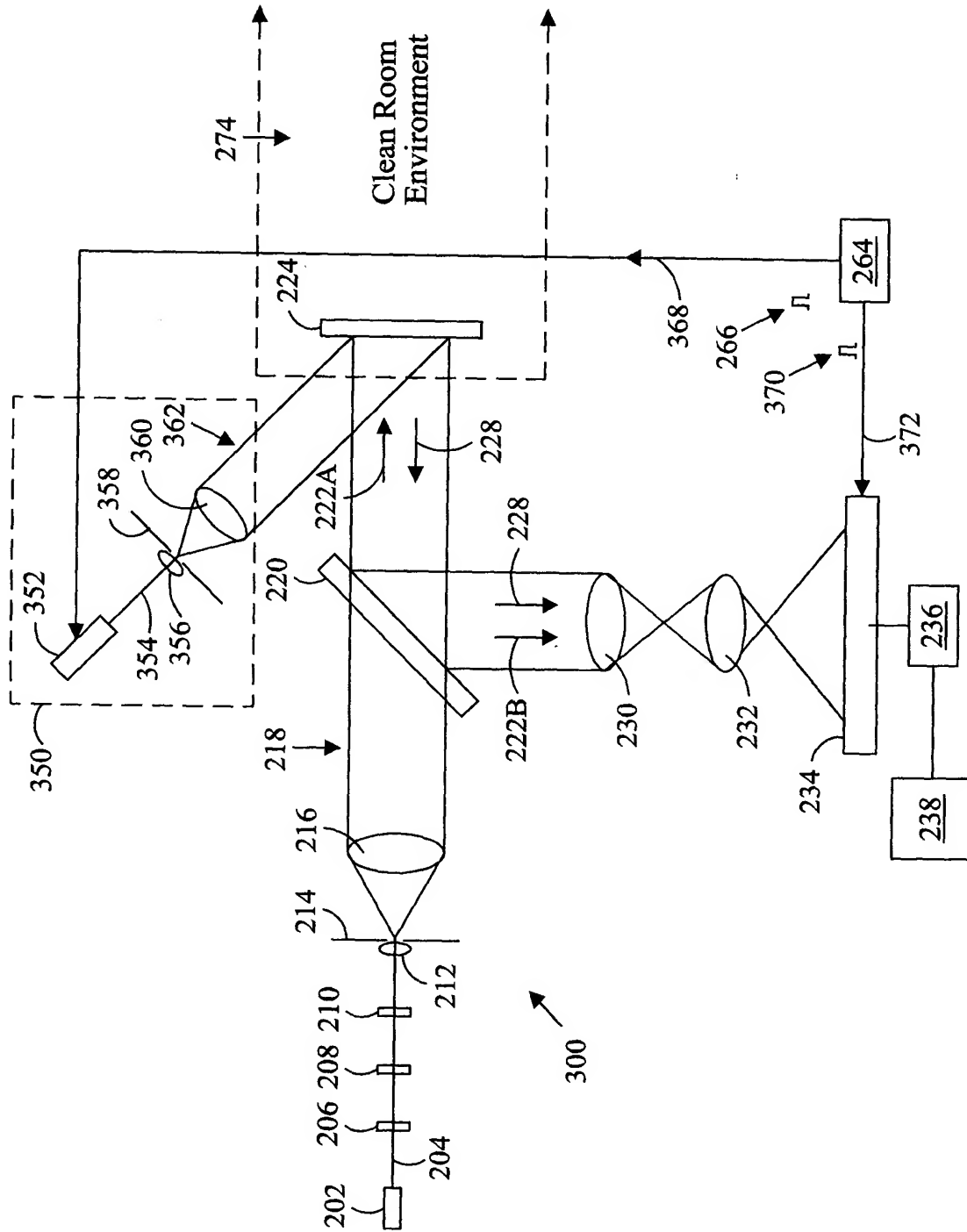


FIG. 7

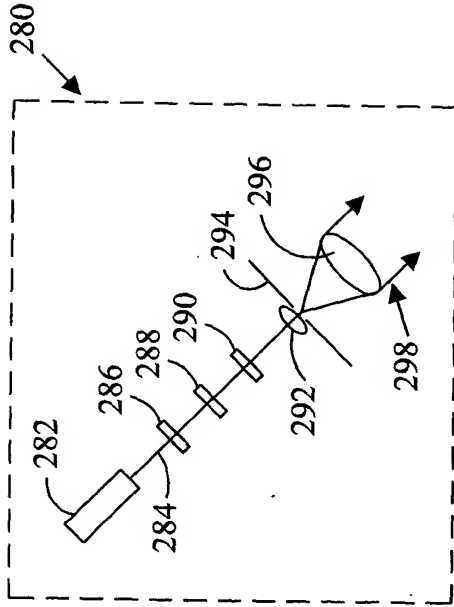


FIG. 8

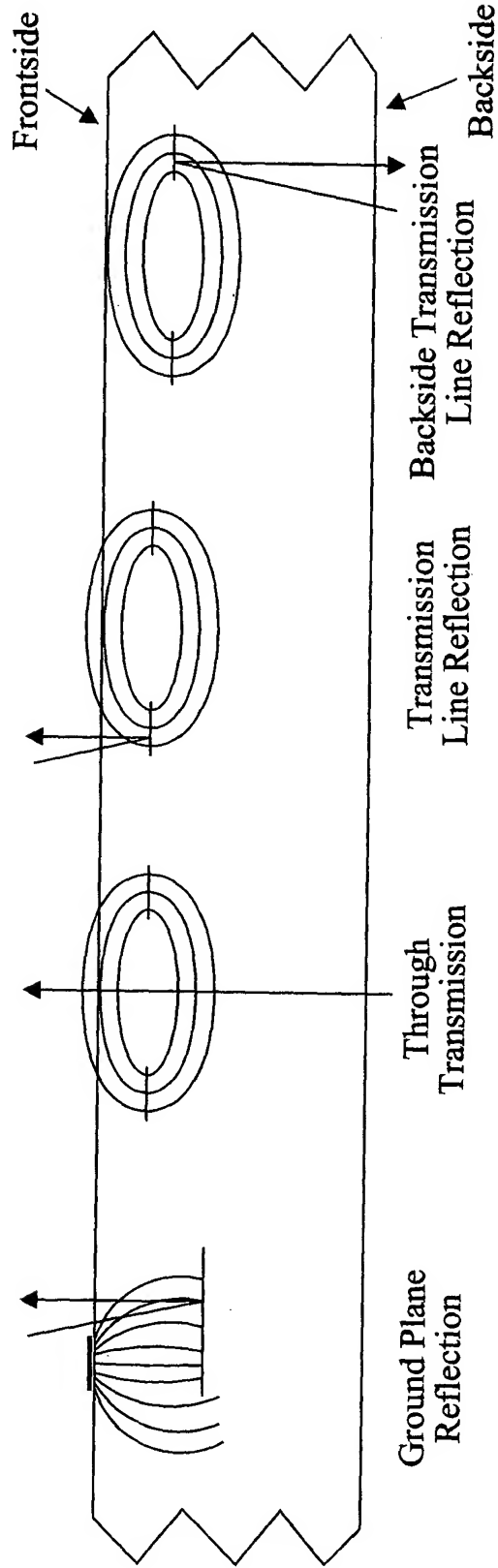


FIG. 9

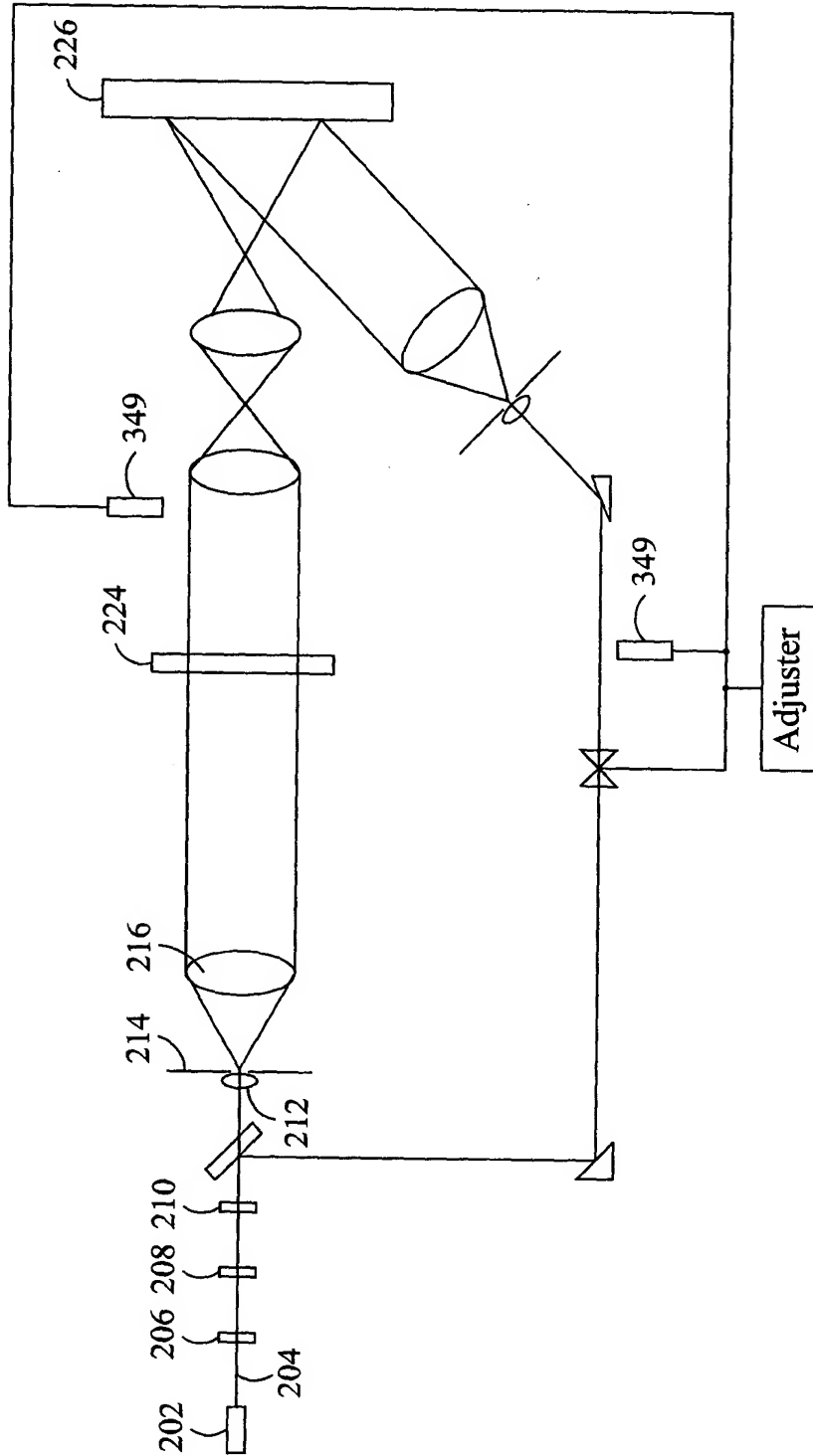


FIG. 10

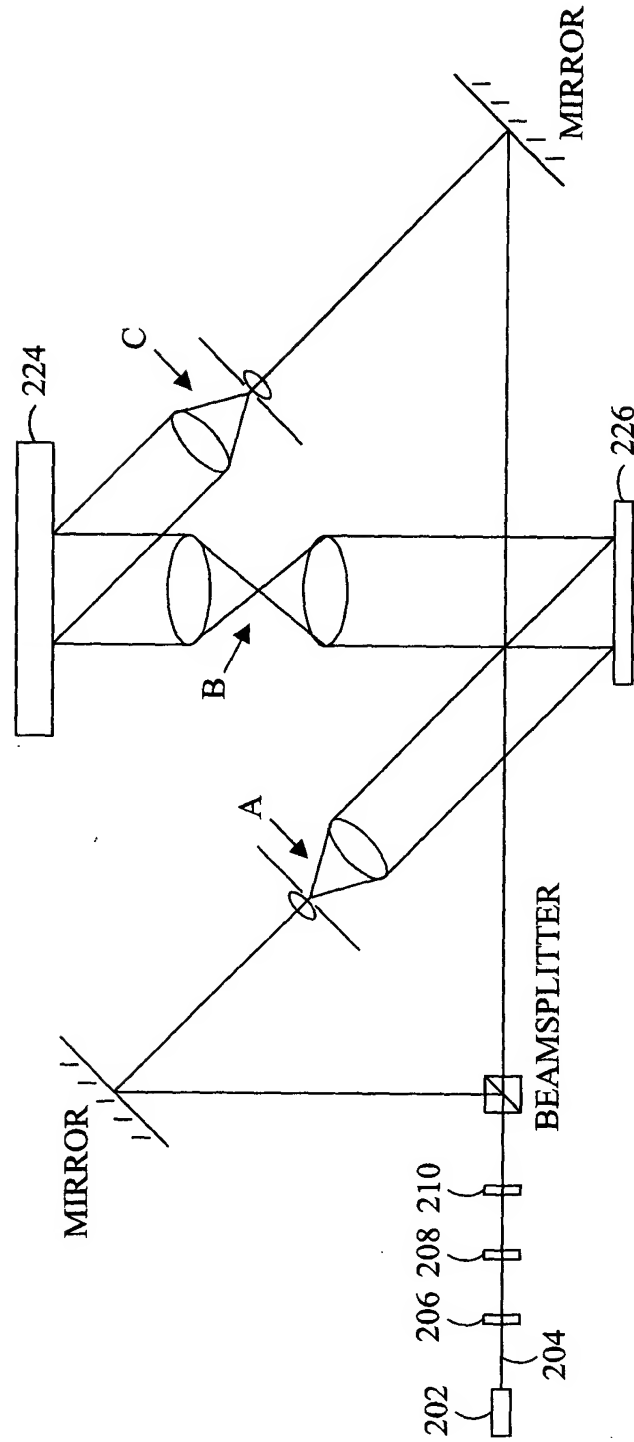


FIG. 11

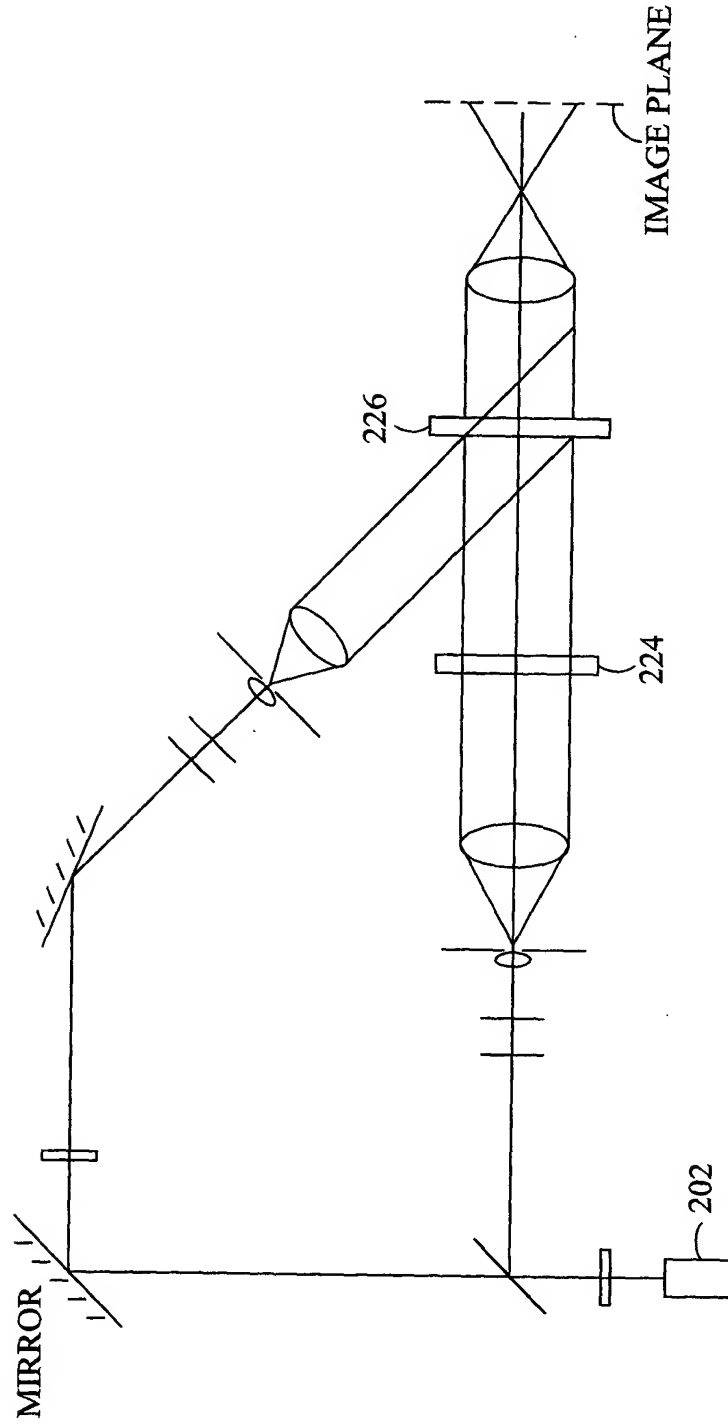


FIG. 12

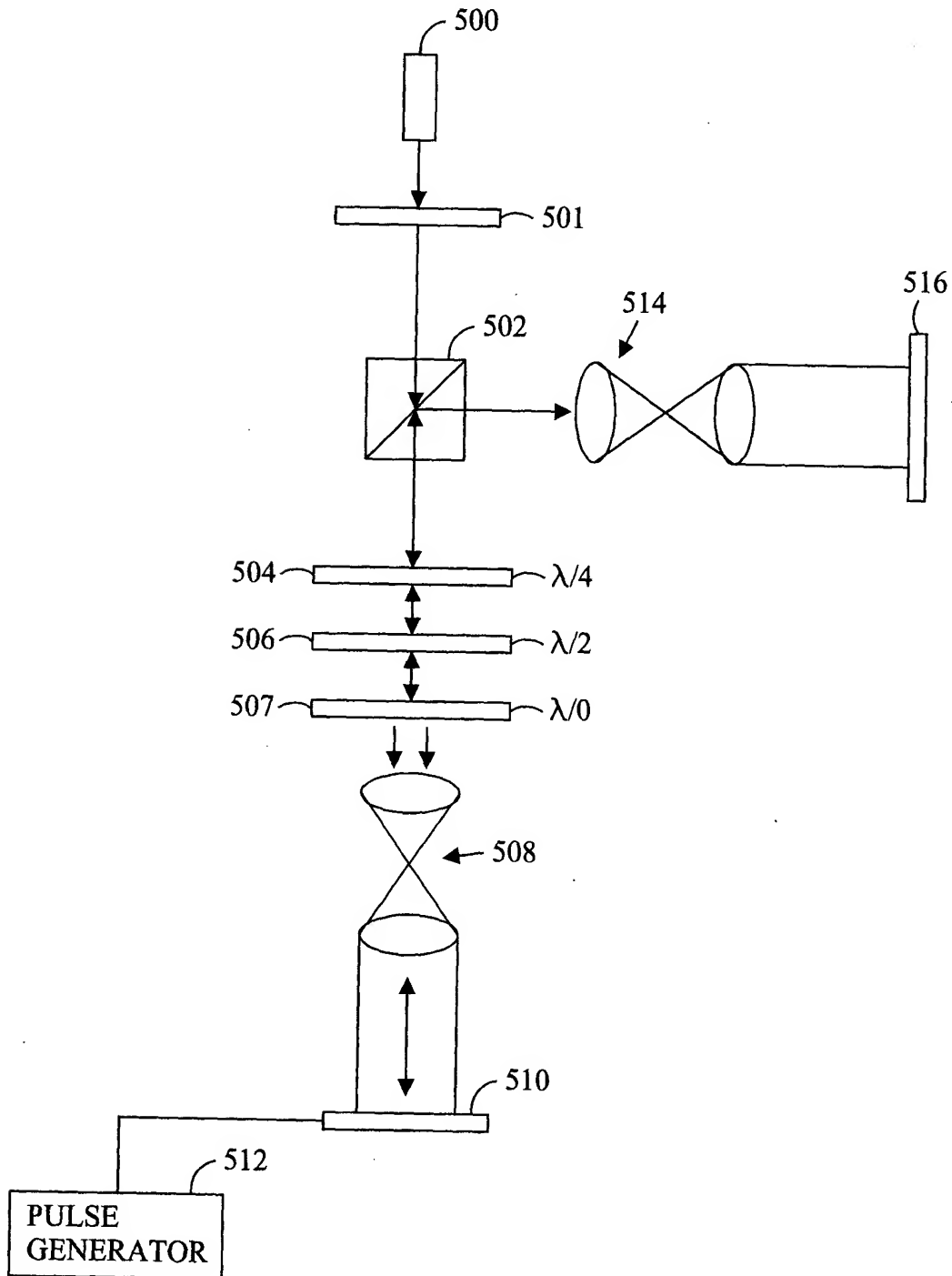


FIG. 13

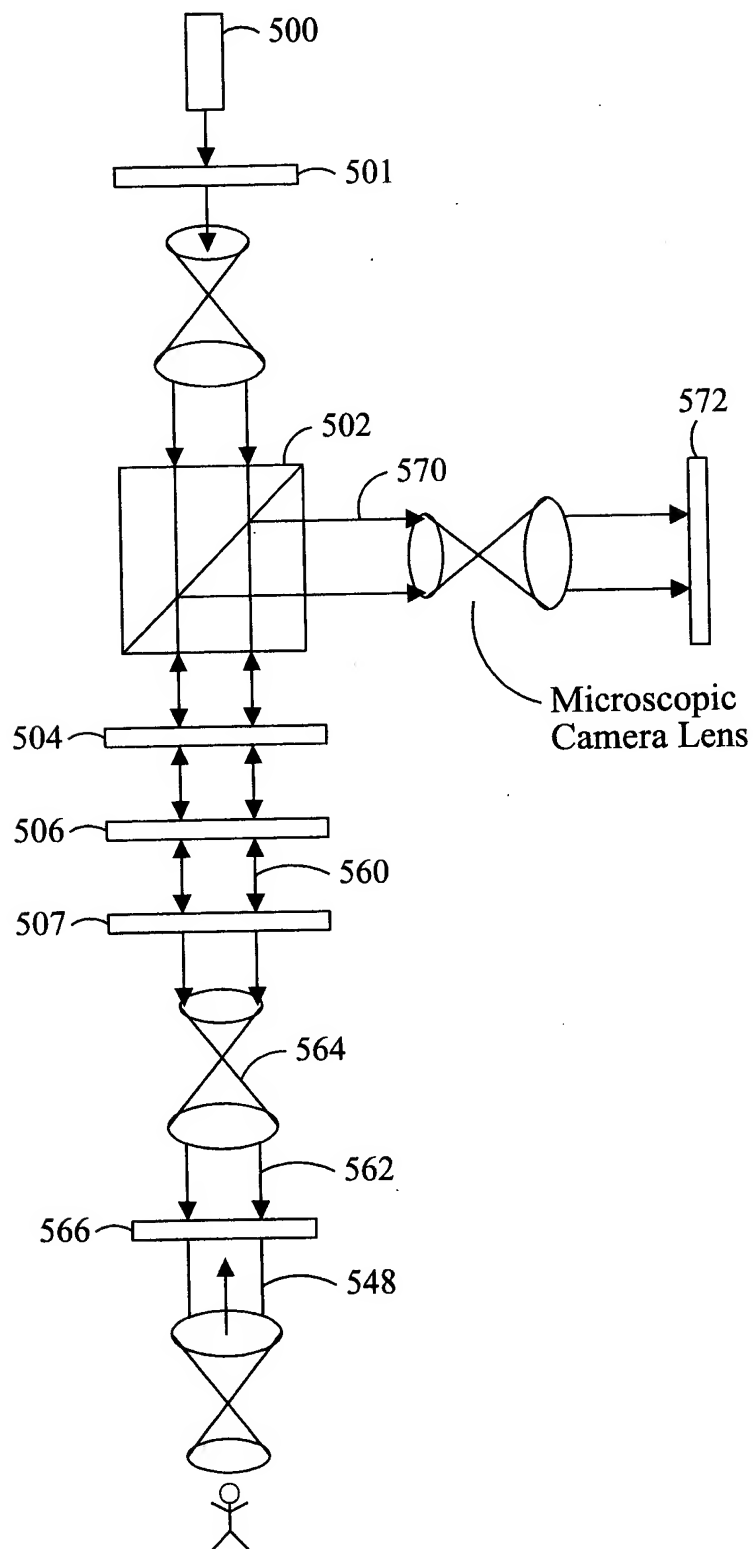


FIG. 14A

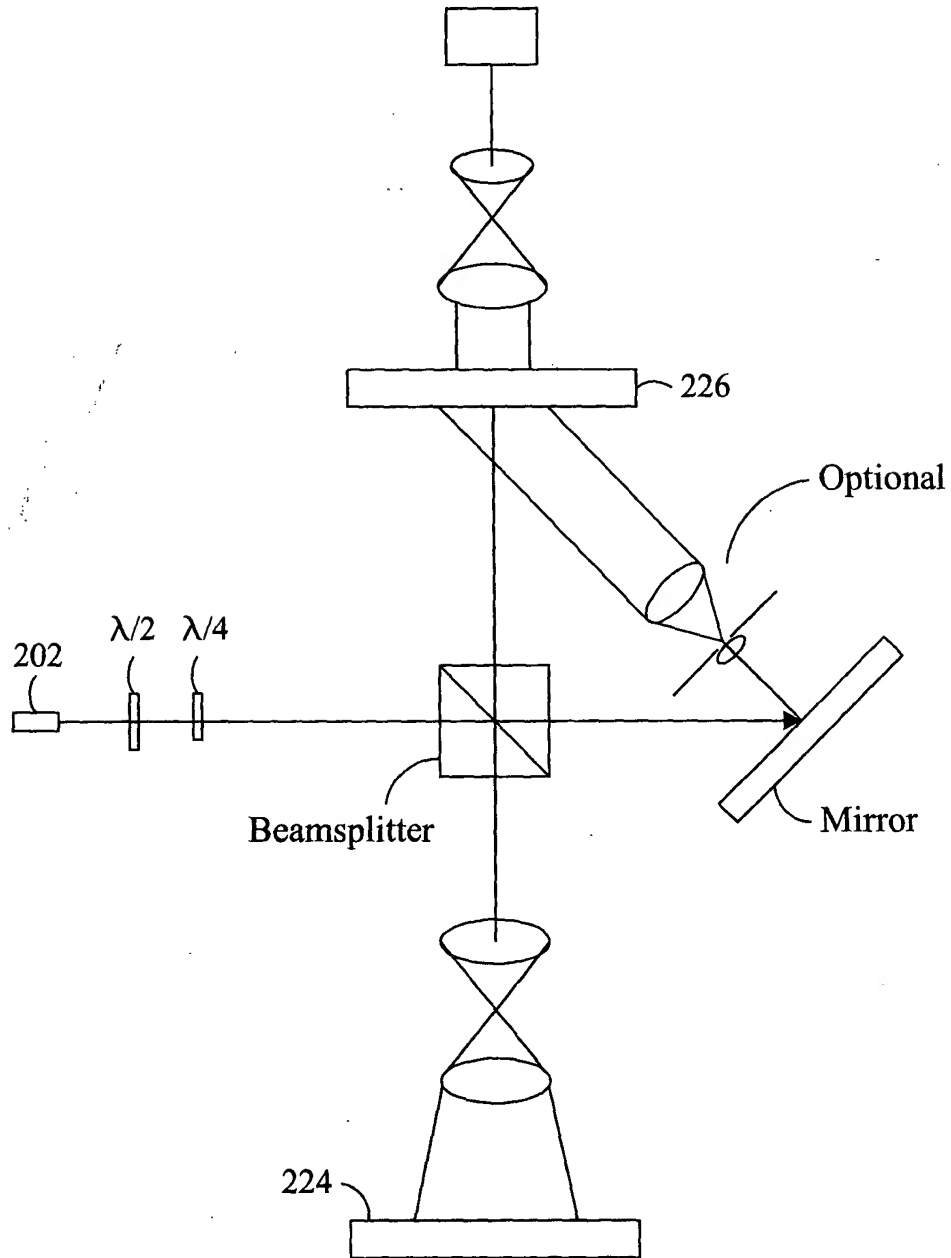


FIG. 14B

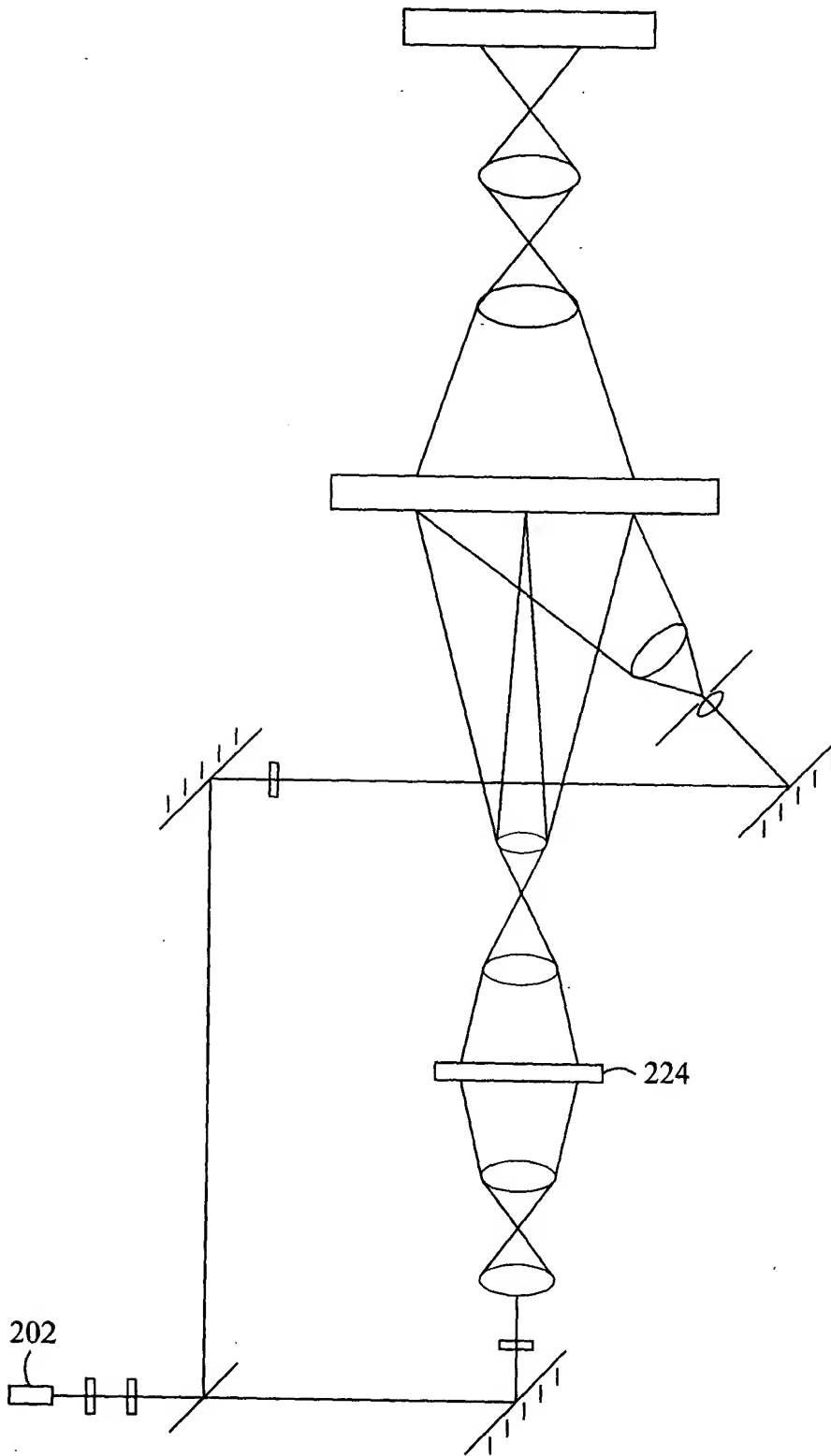
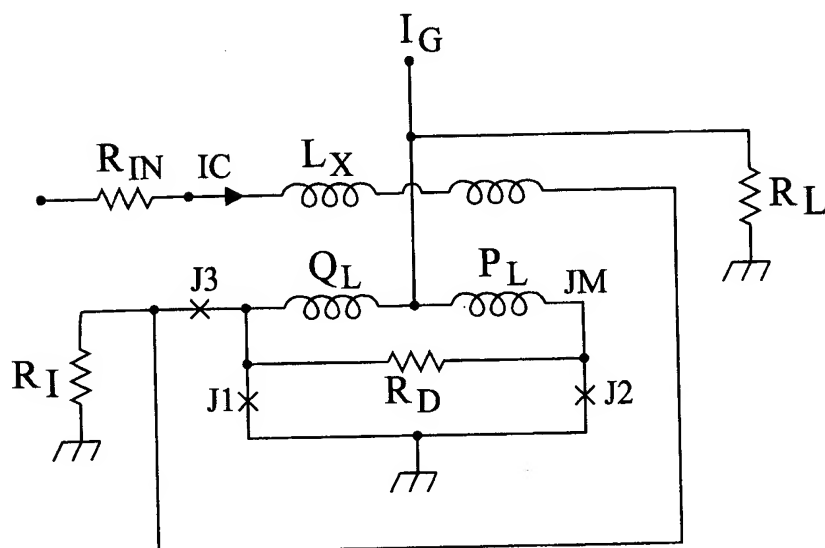
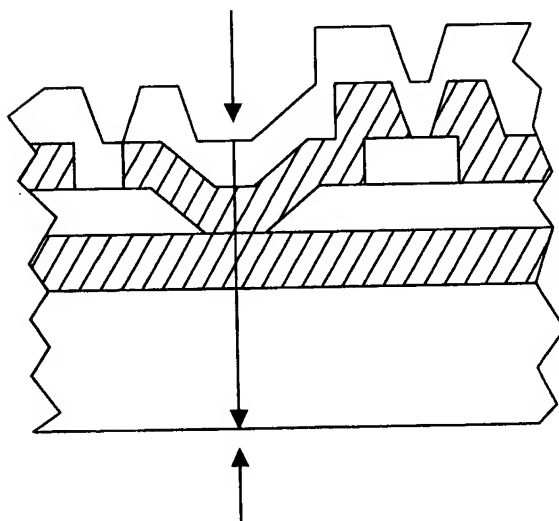


FIG. 14C



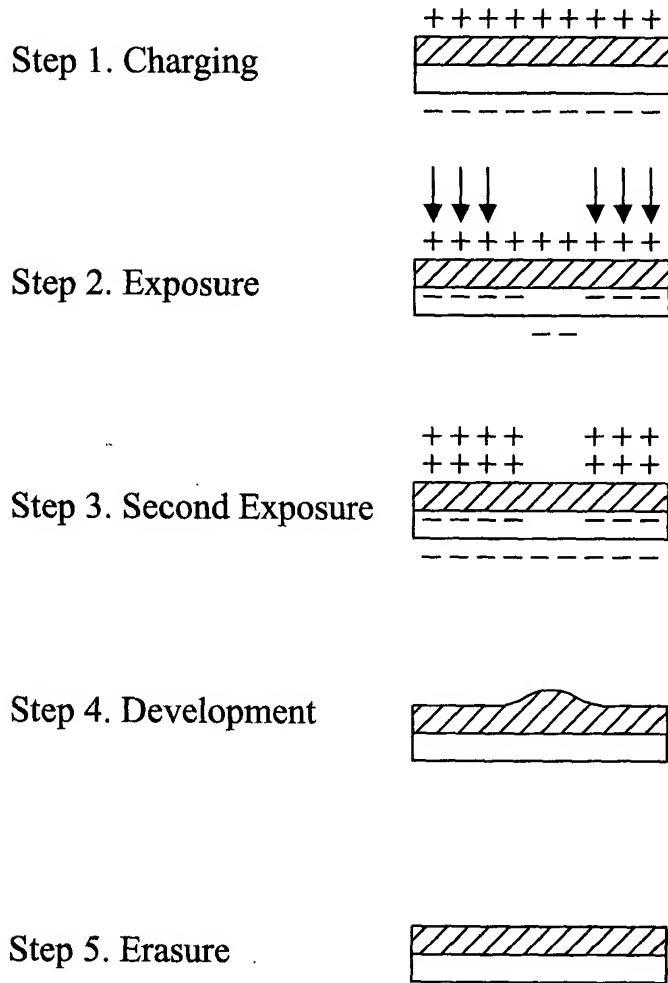
Circuit of Refractory Josephson OR Gate

FIG. 15A



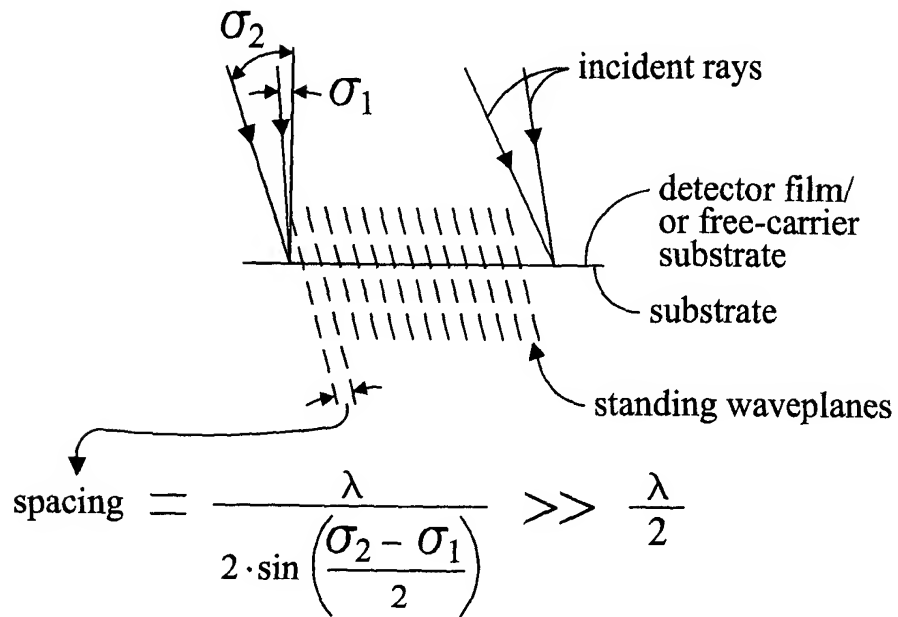
IC crosscut showing Josephson Gate/Junction and area of non-invasive Holographic microscopic inspection using arrangements disclosed.

FIG. 15B



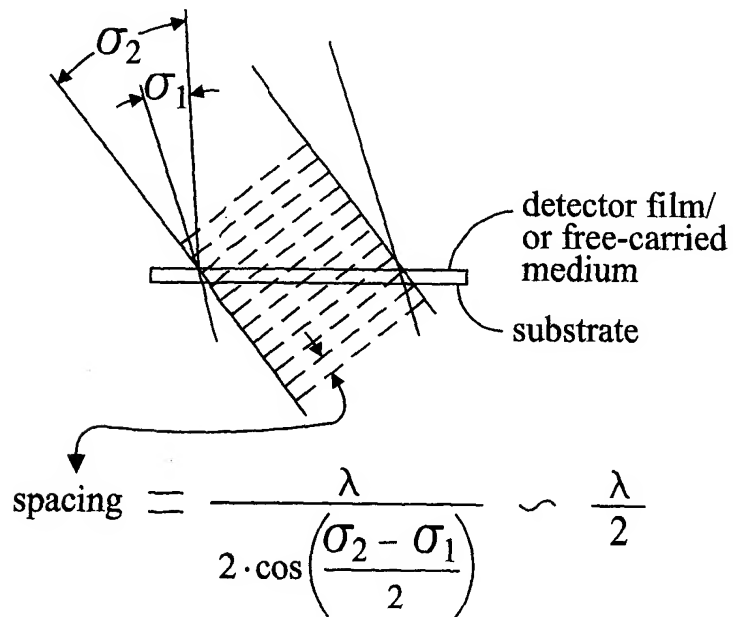
Record-erase cycle for an IR Thermoplastic recording material

FIG. 16



Conventional Method
(single sided Hologram/Interferogram)

FIG. 16A



Double Sided Method
(Holography/Interferogram)

FIG. 16B



FIG. 17

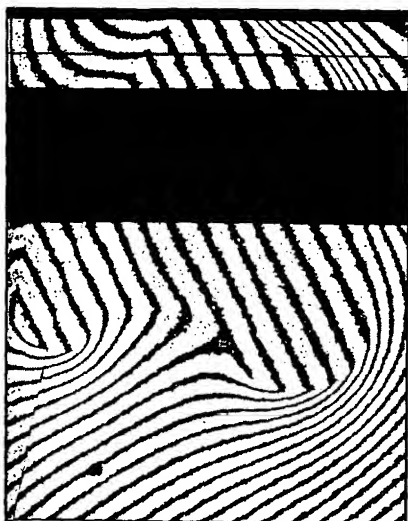


FIG. 18

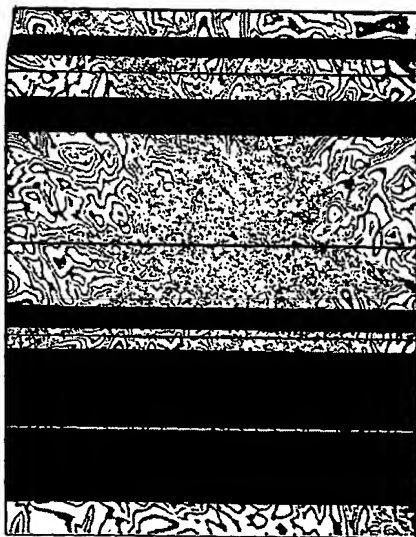


FIG. 19

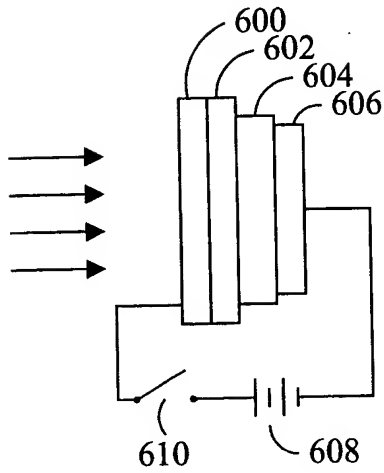


FIG. 20

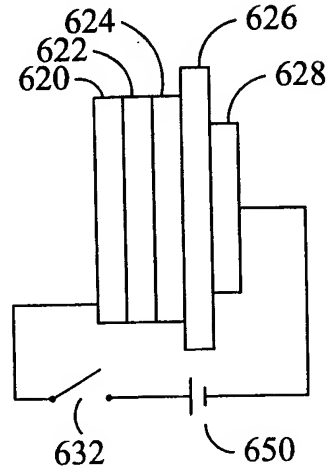


FIG. 21

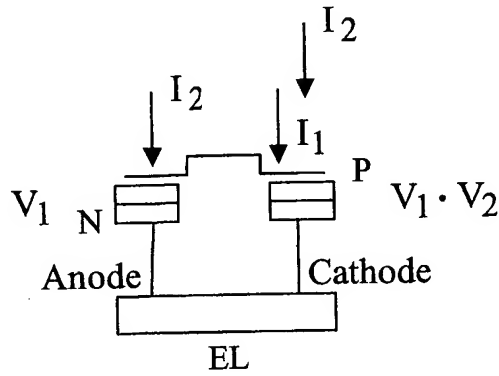


FIG. 22

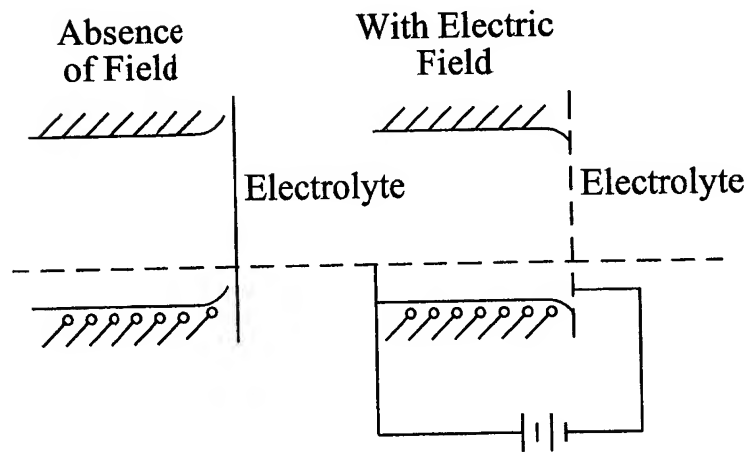


FIG. 23

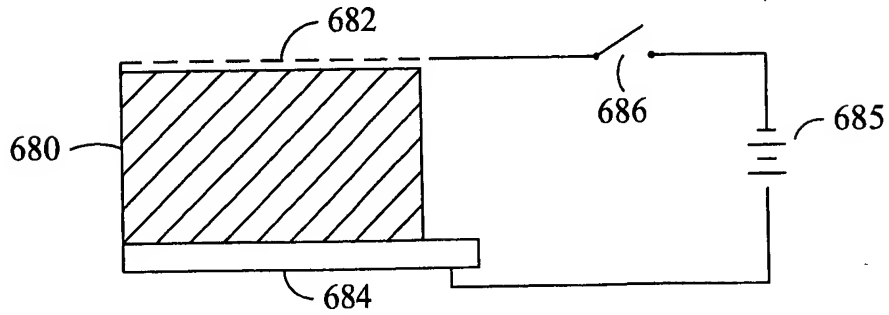


FIG. 24

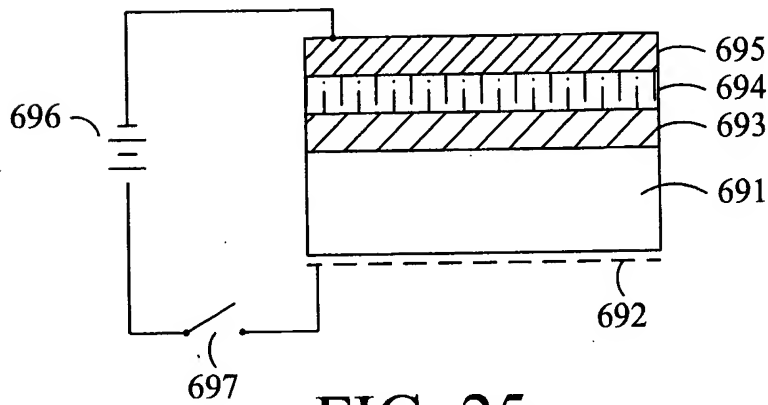


FIG. 25

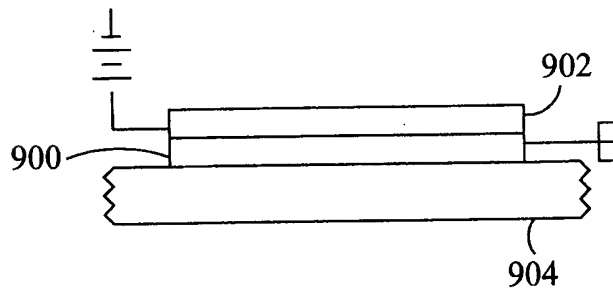


FIG. 26A

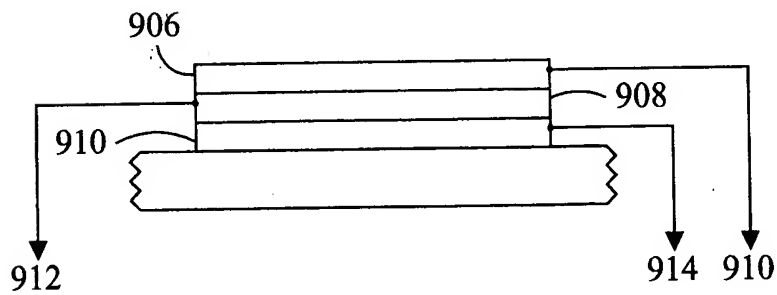


FIG. 26B

Semiconductor layer and orientation thickness of
P-N materials corresponds to standing waveplanes
in single-sided free-carrier IR Holography

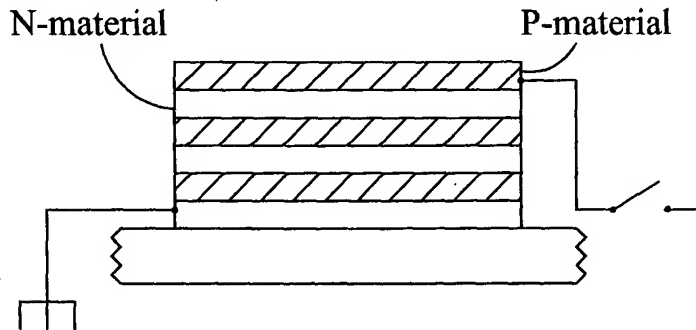


FIG. 27A

Semiconductor orientation and the column dimensions
dimensions corresponds to standing waveplanes
in double-sided free-carrier IR Holography
(Refer to FIG. 16A and 16B as well as FIG. 27A)

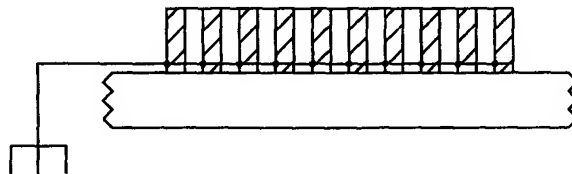


FIG. 27B

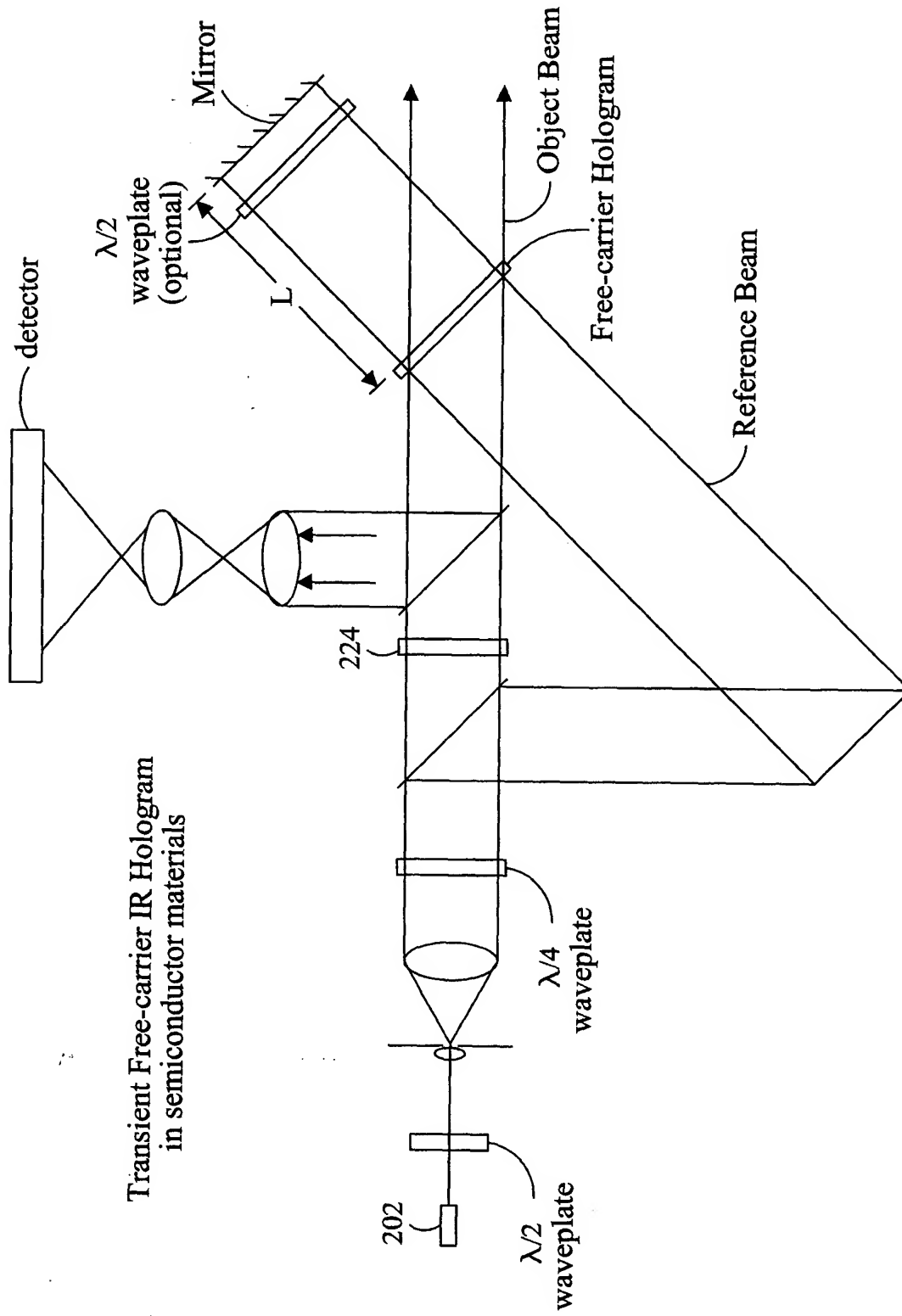


FIG. 28

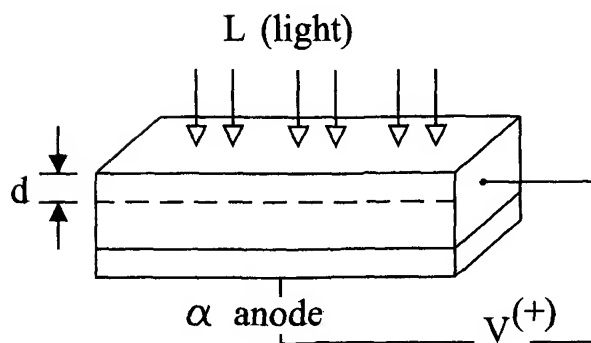


FIG. 29

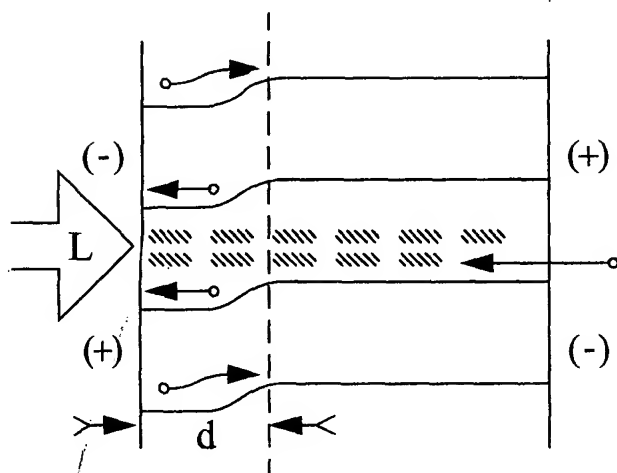


FIG. 30

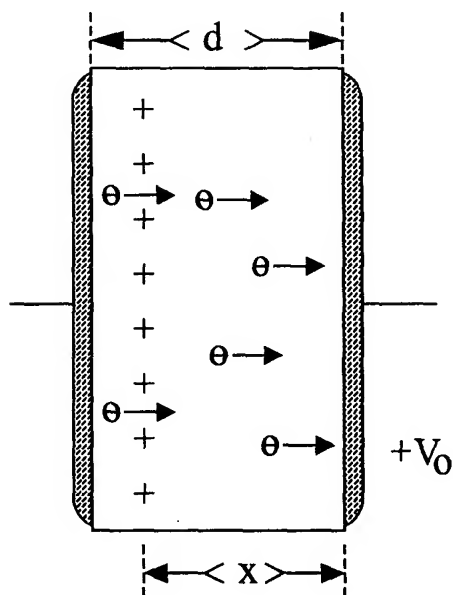
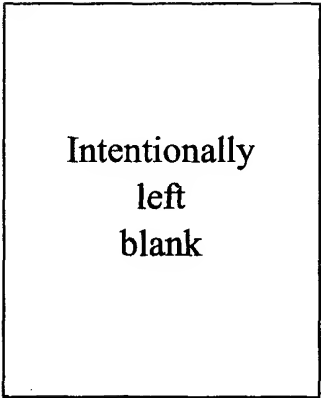


FIG. 31



Intentionally
left
blank

FIG. 32

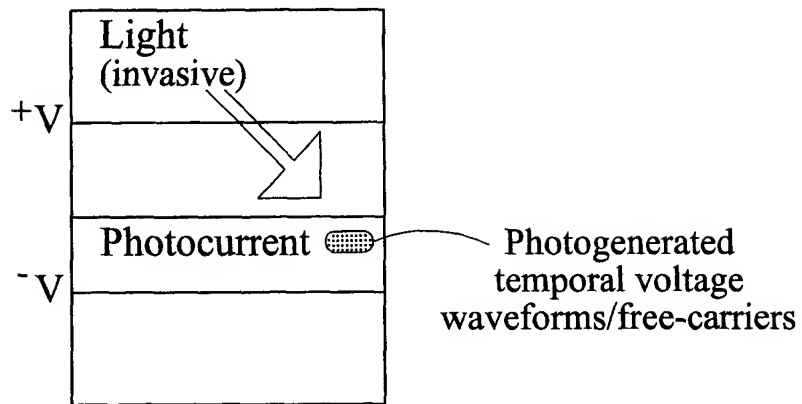


FIG. 33

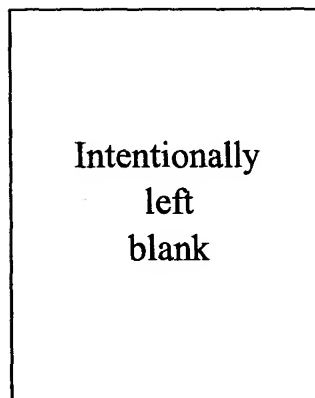


FIG. 34

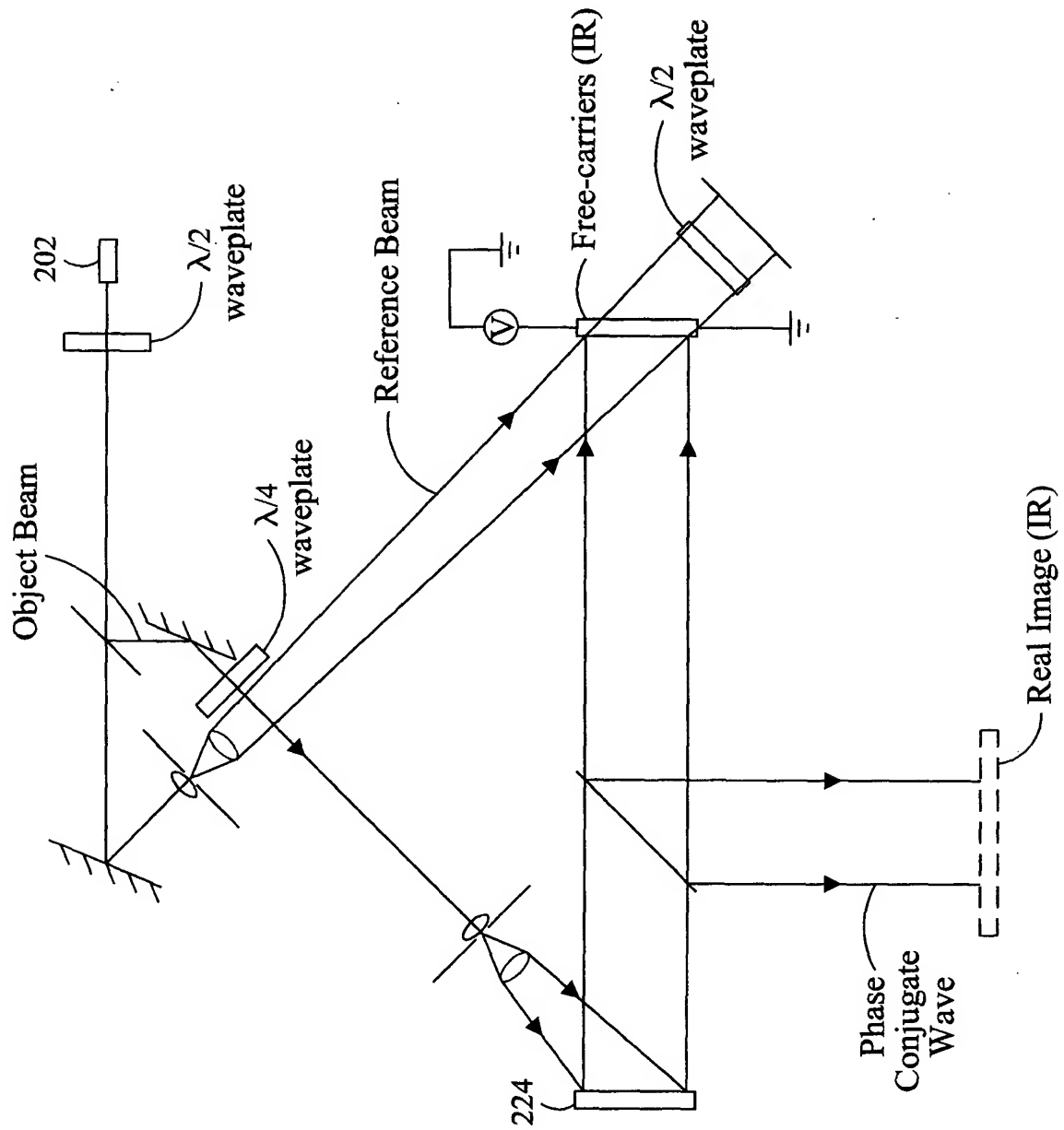


FIG. 35

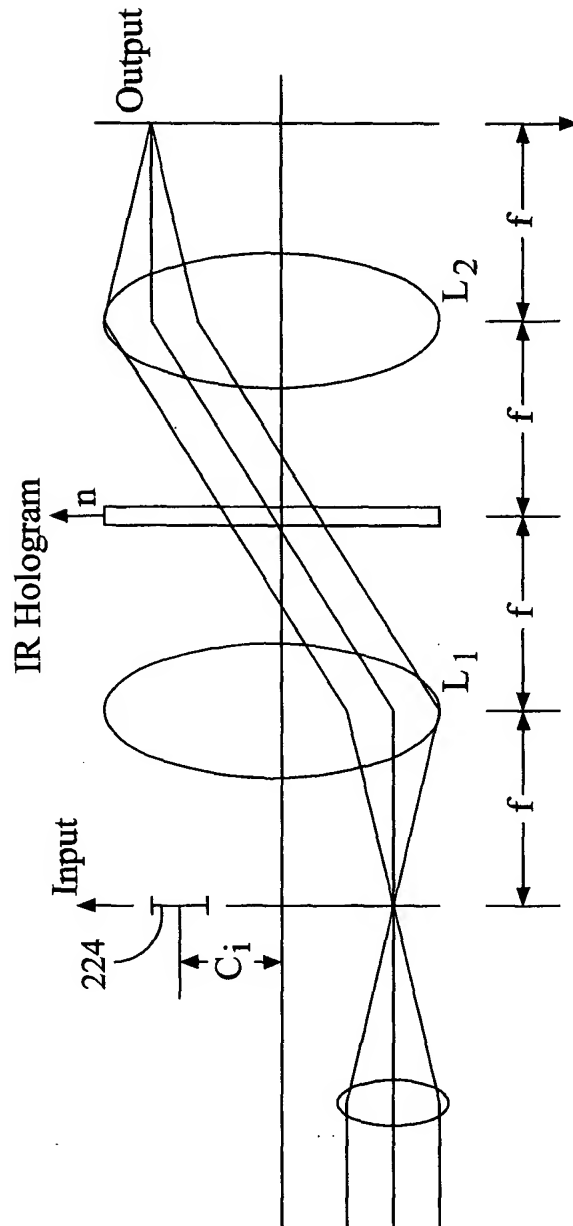


FIG. 36

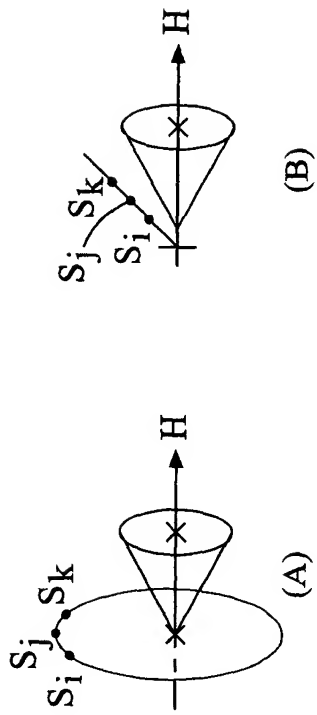


FIG. 37A

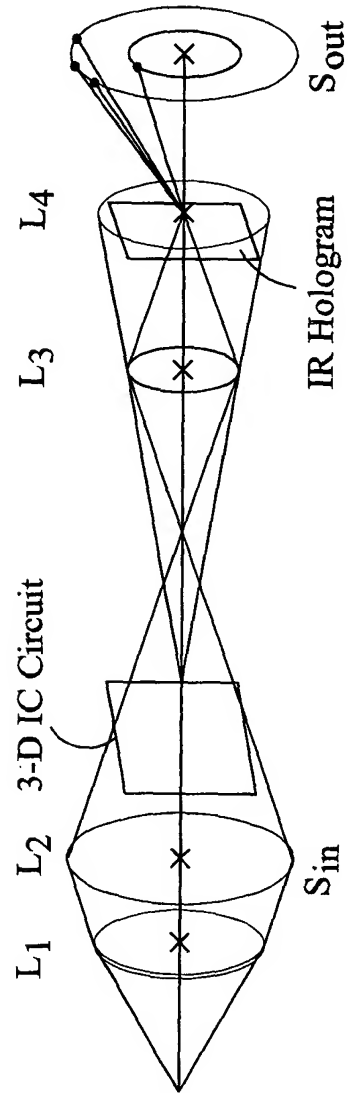


FIG. 37B

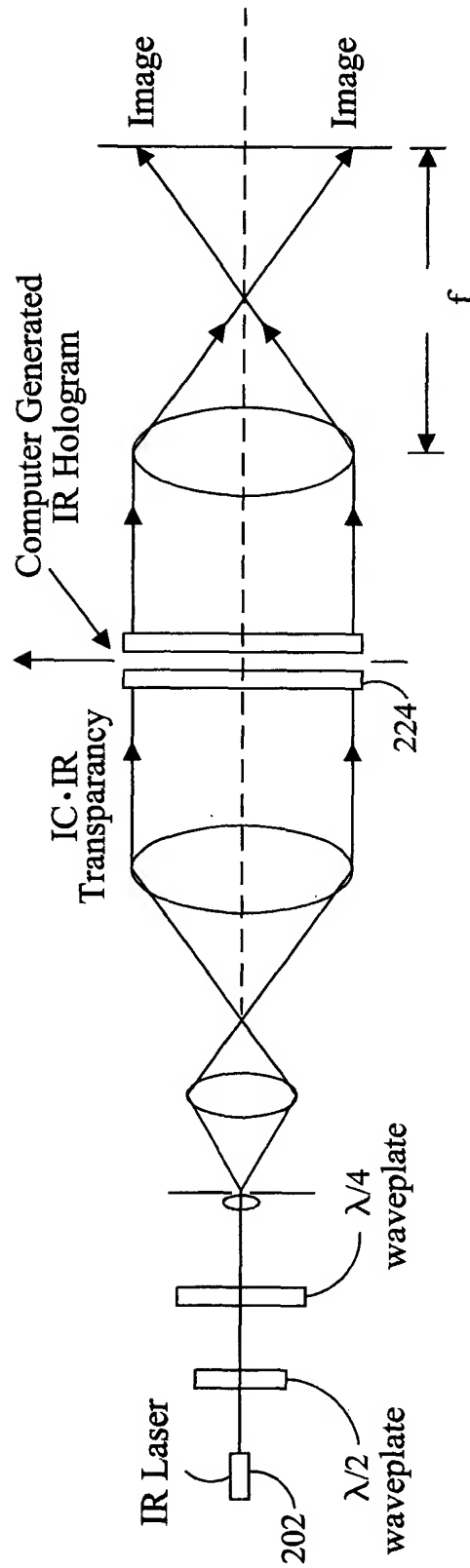


FIG. 38

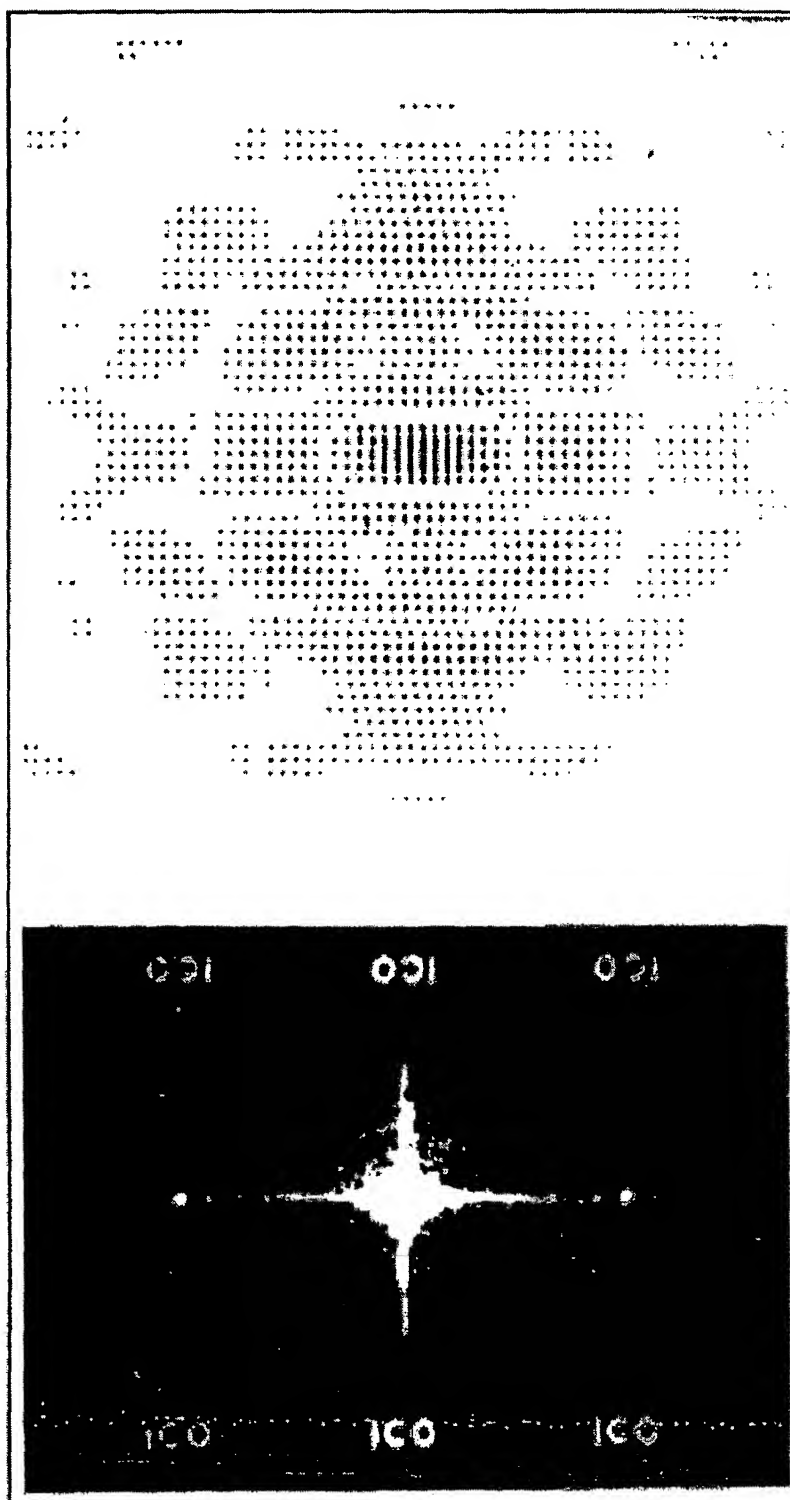


FIG. 39

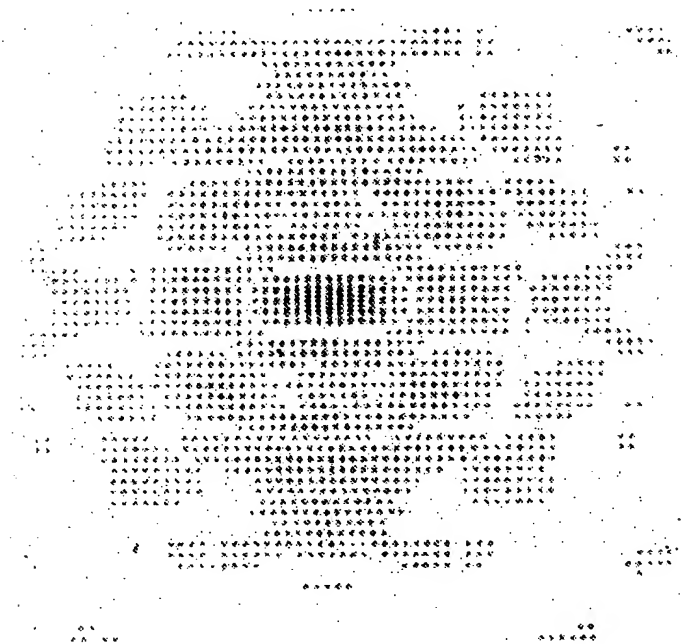


FIG. 40A

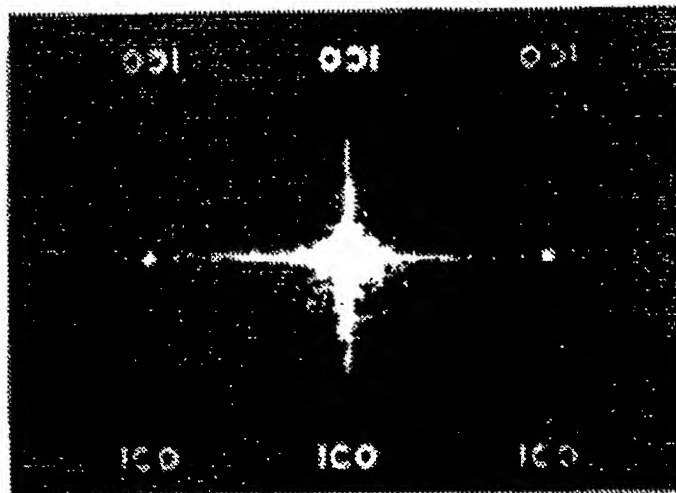


FIG. 40B

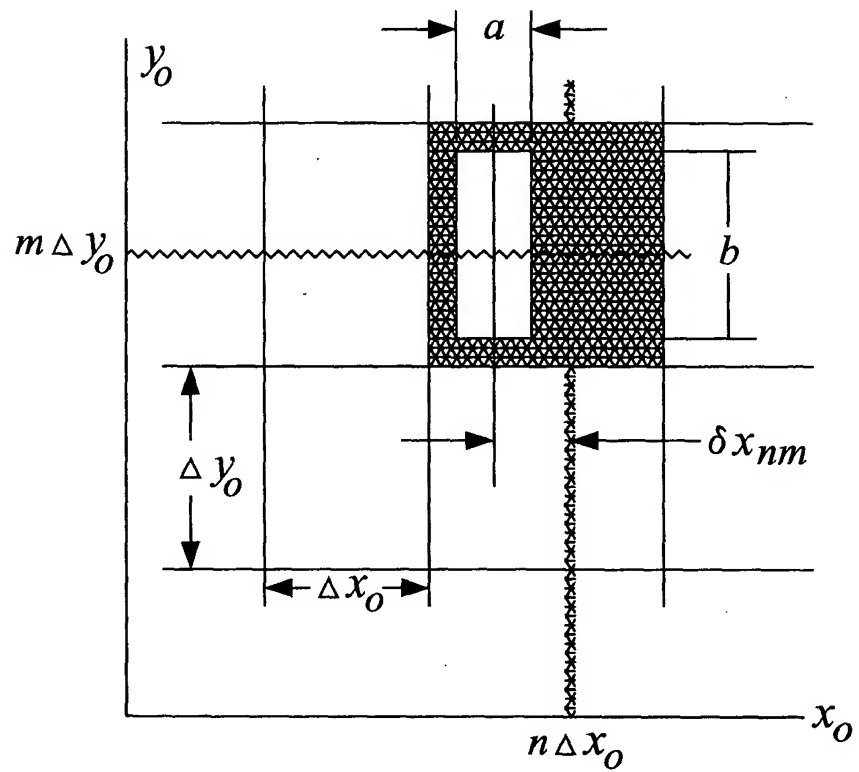


FIG. 40C

Invention: VOLTAGE TESTING AND MEASUREMENT

Filed: Concurrently herewith Attorney: Kevin L. Russell, Reg. No. 38,292
Inventors: Pfaff, et al. Telephone: (503) 227-5631

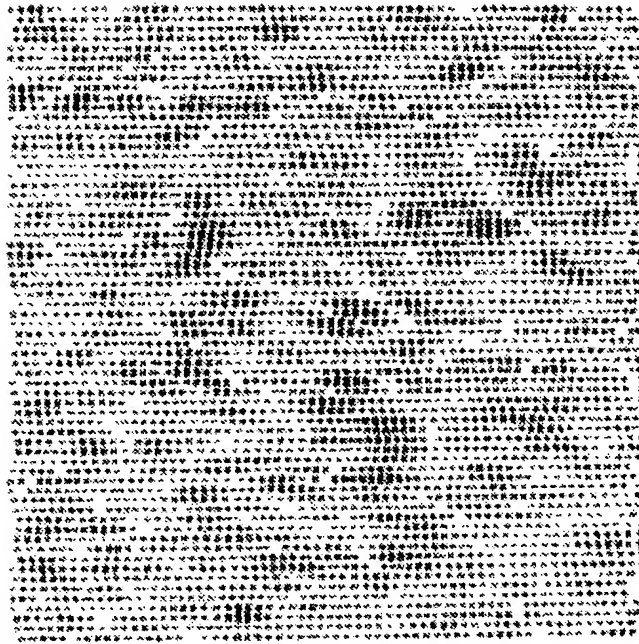


FIG. 41A



FIG. 41B

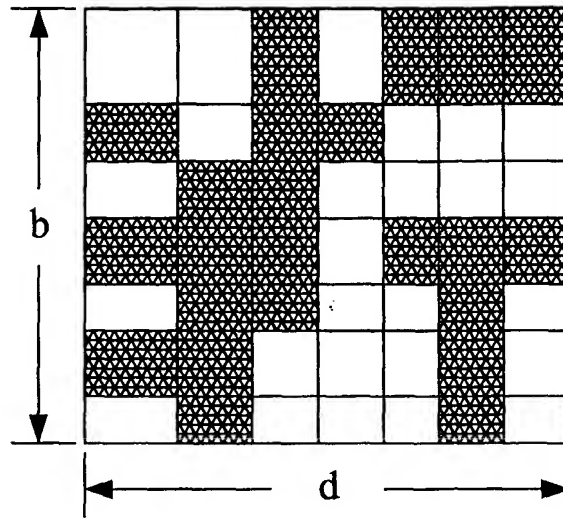
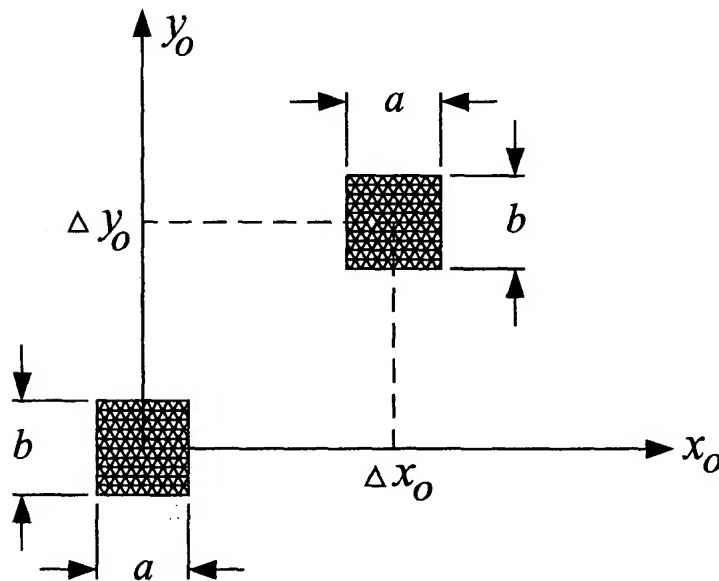


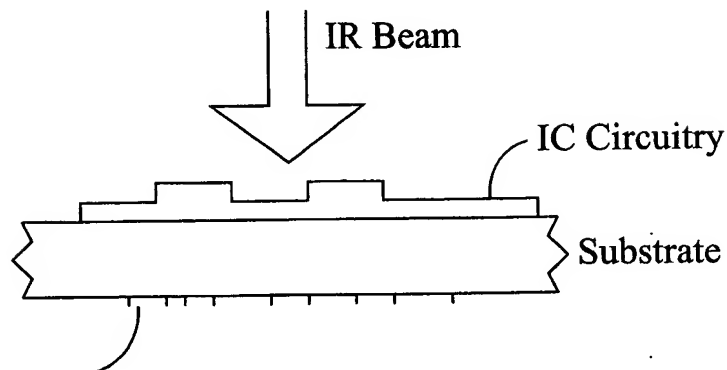
Illustration showing arrangement of generalized Gunary detour-phase IR Hologram

FIG. 42

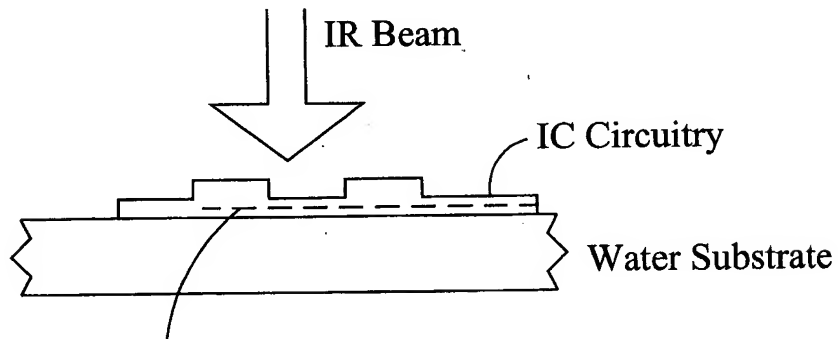


IR Diffraction at a Rectangular Aperture

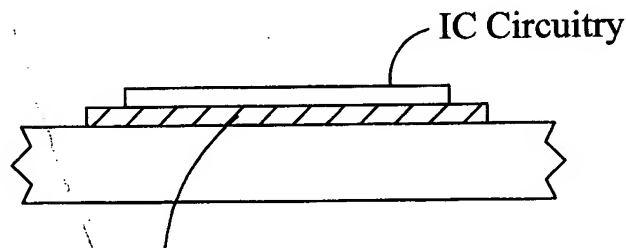
FIG. 43



IR Hologram printed on back, computer generated or directly exposed for testing of IC functionality



HOE - IR Holographic Optical Element built directly into IC's circuitry gives optimal interferogram if IC lithography and operating voltage parameters are okay. Can also be set up to detect failure conditions or other operations.



IR computer generated Hologram can also be ion-beam etched/implanted into wafer substrate.

FIG. 44